

Fig. 1

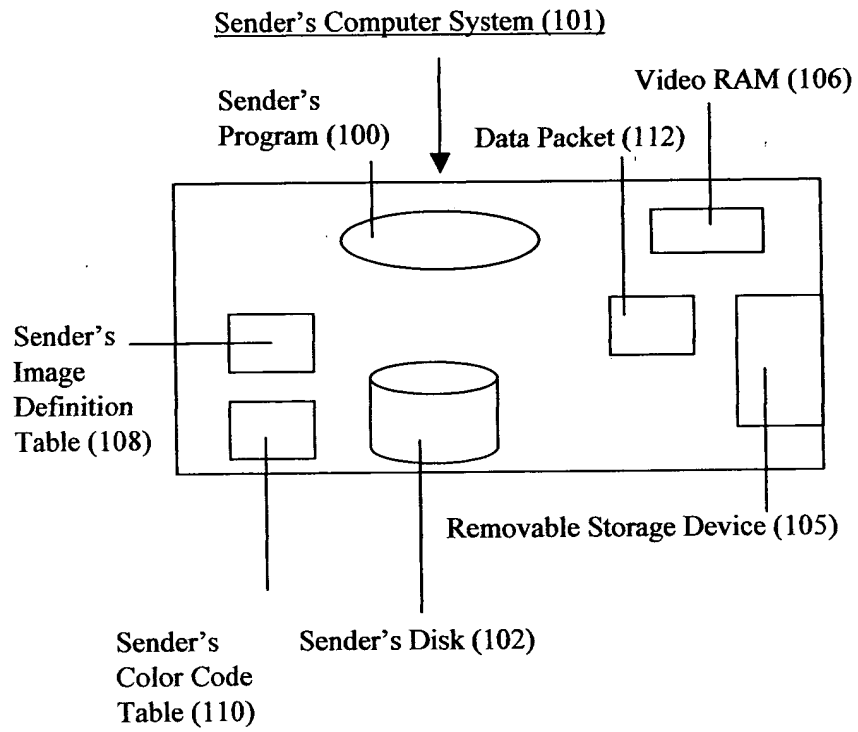


Fig. 1a

3/16

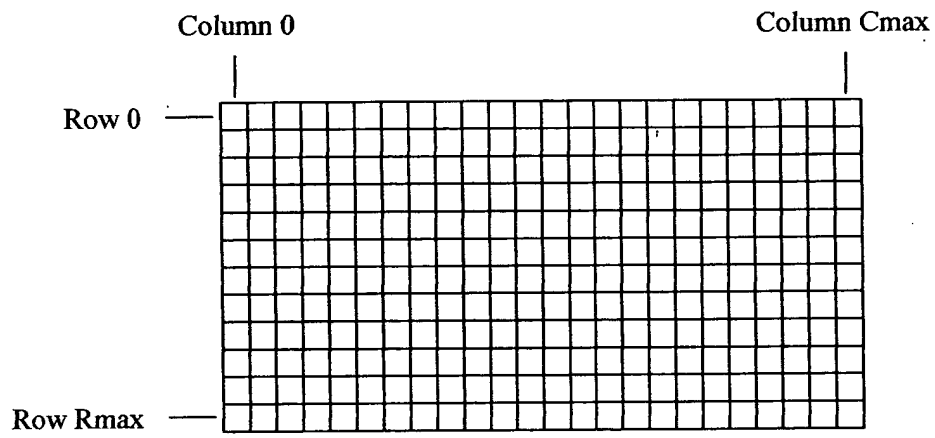


Fig. 2

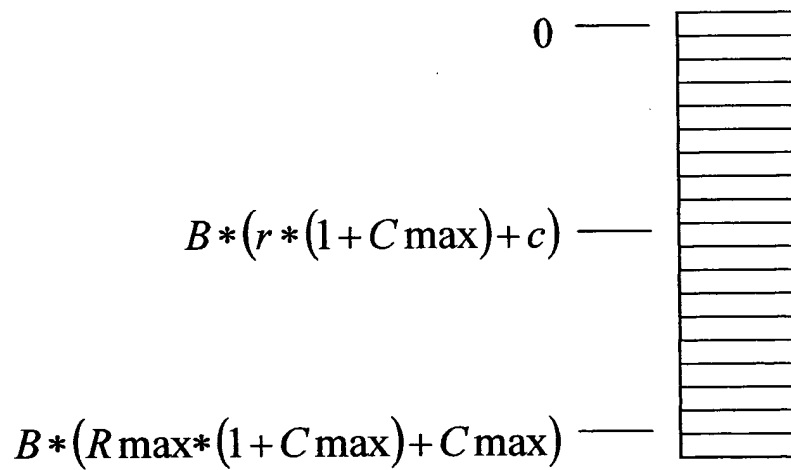


Fig. 3

4/16

<u>Image Area</u>	<u>Ordered Set of Memory Address Offsets</u>
0	{ Set 0 }
1	{ Set 1 }
2	{ Set 2 }
Amax	{ Set Amax }

Fig. 4

<u>Row</u>	<u>Red</u>	<u>Green</u>	<u>Blue</u>	<u>Color Value</u>
0	r0	g0	b0	c0
1	r1	g1	b1	c1
2	r2	g2	b2	c2
..				
..				
..				
2 ^N - 1				

Fig. 5

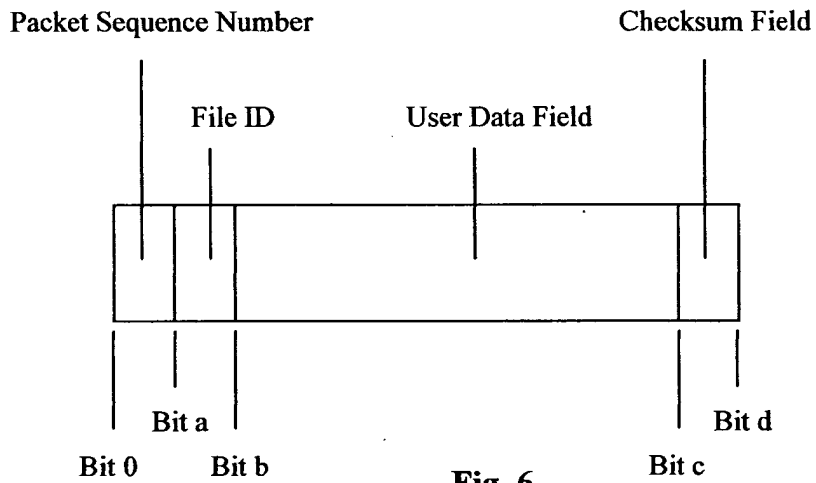


Fig. 6

5/16

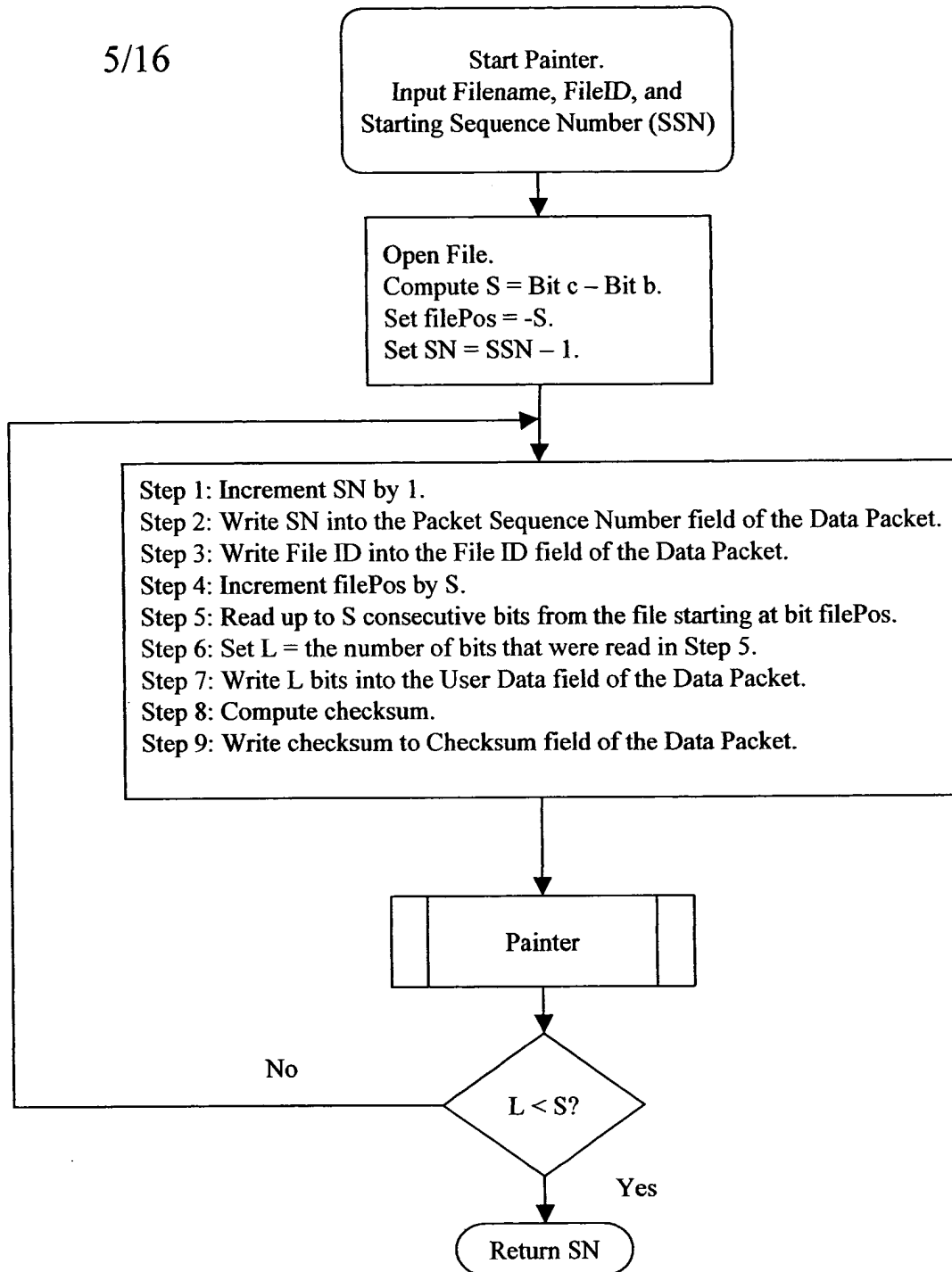


Fig. 7

6/16

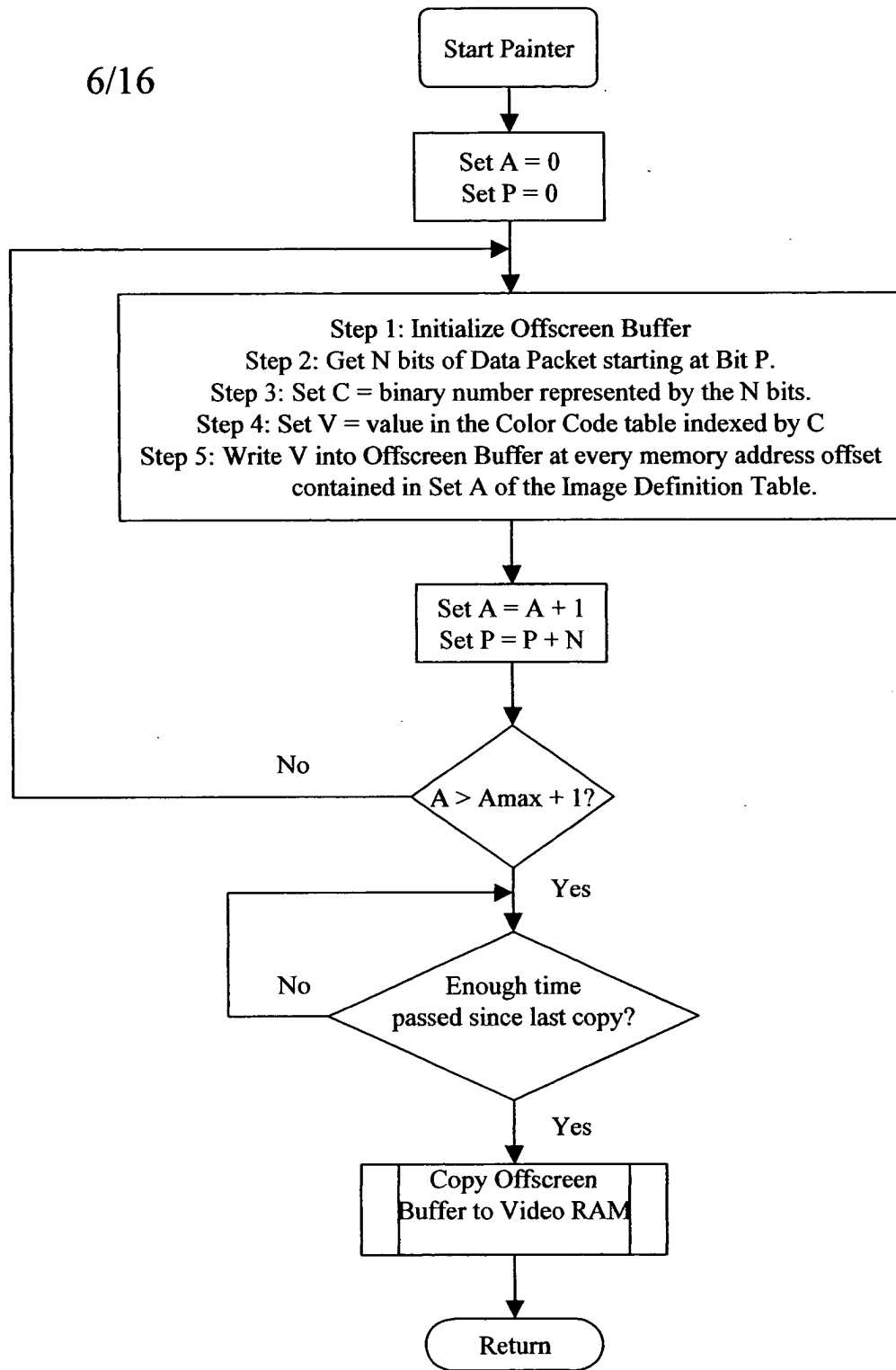


Fig. 8

7/16

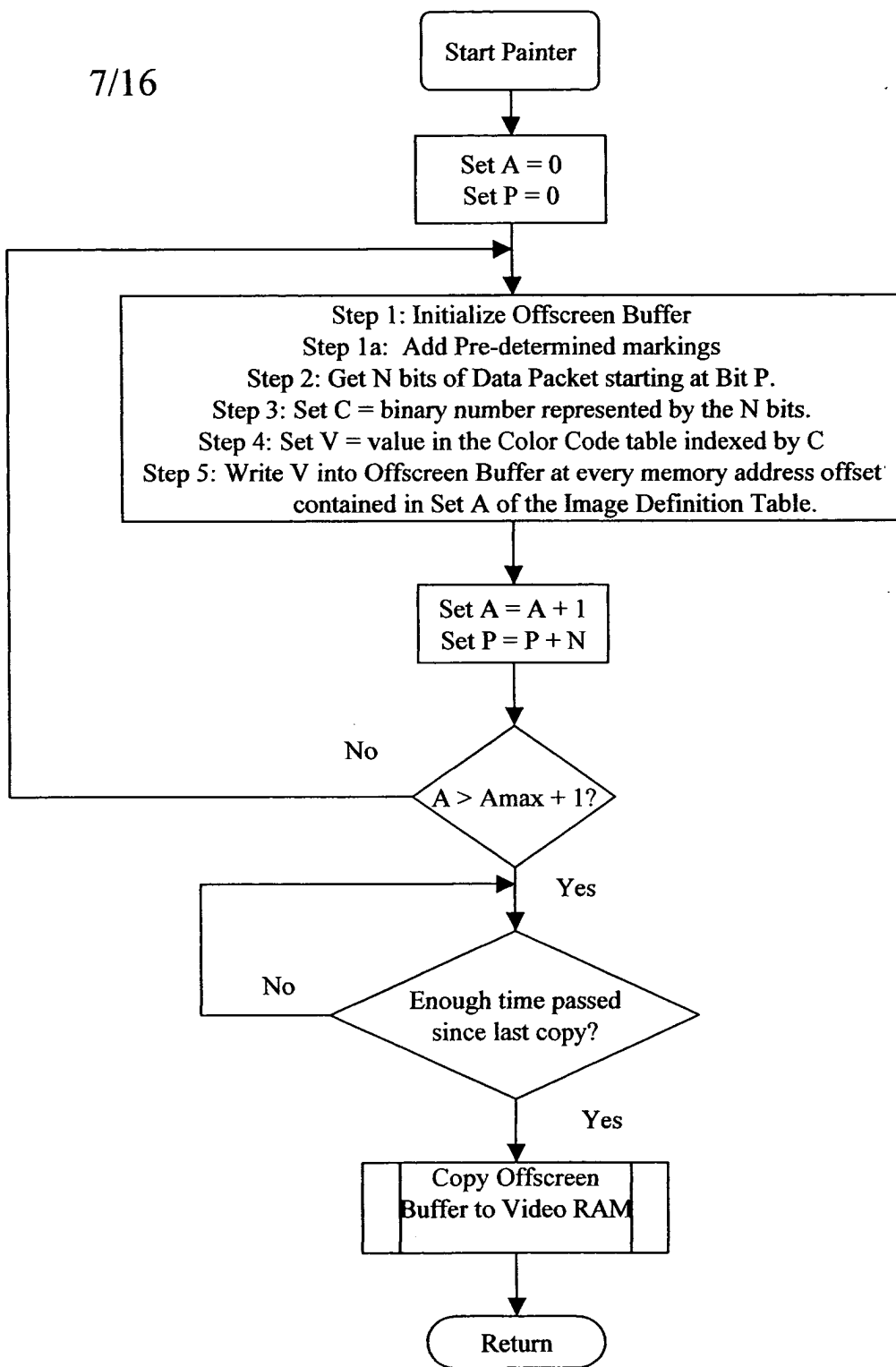


Fig. 8a

8/16

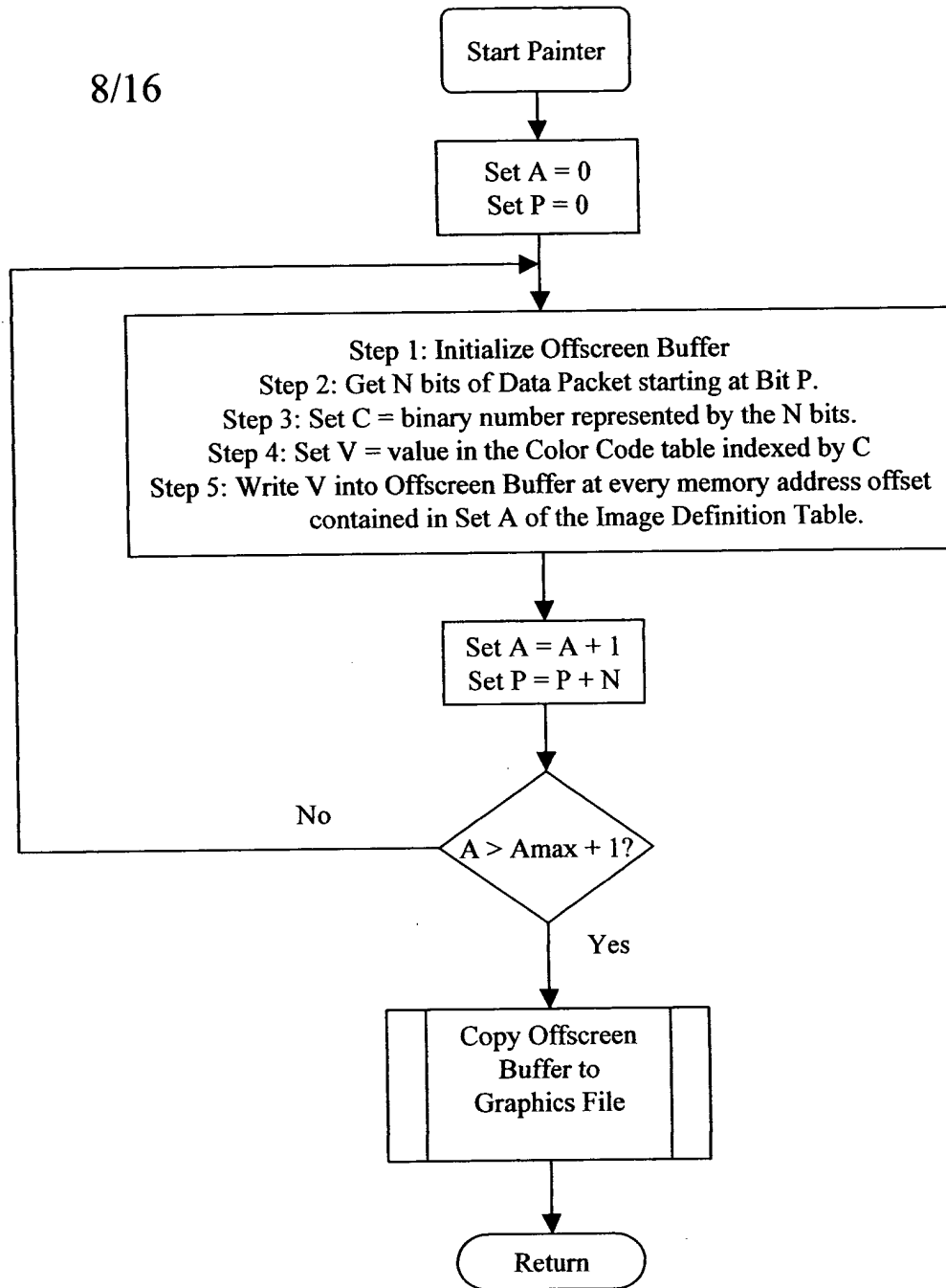


Fig. 8b

9/16 Receiver's Computer System (201)

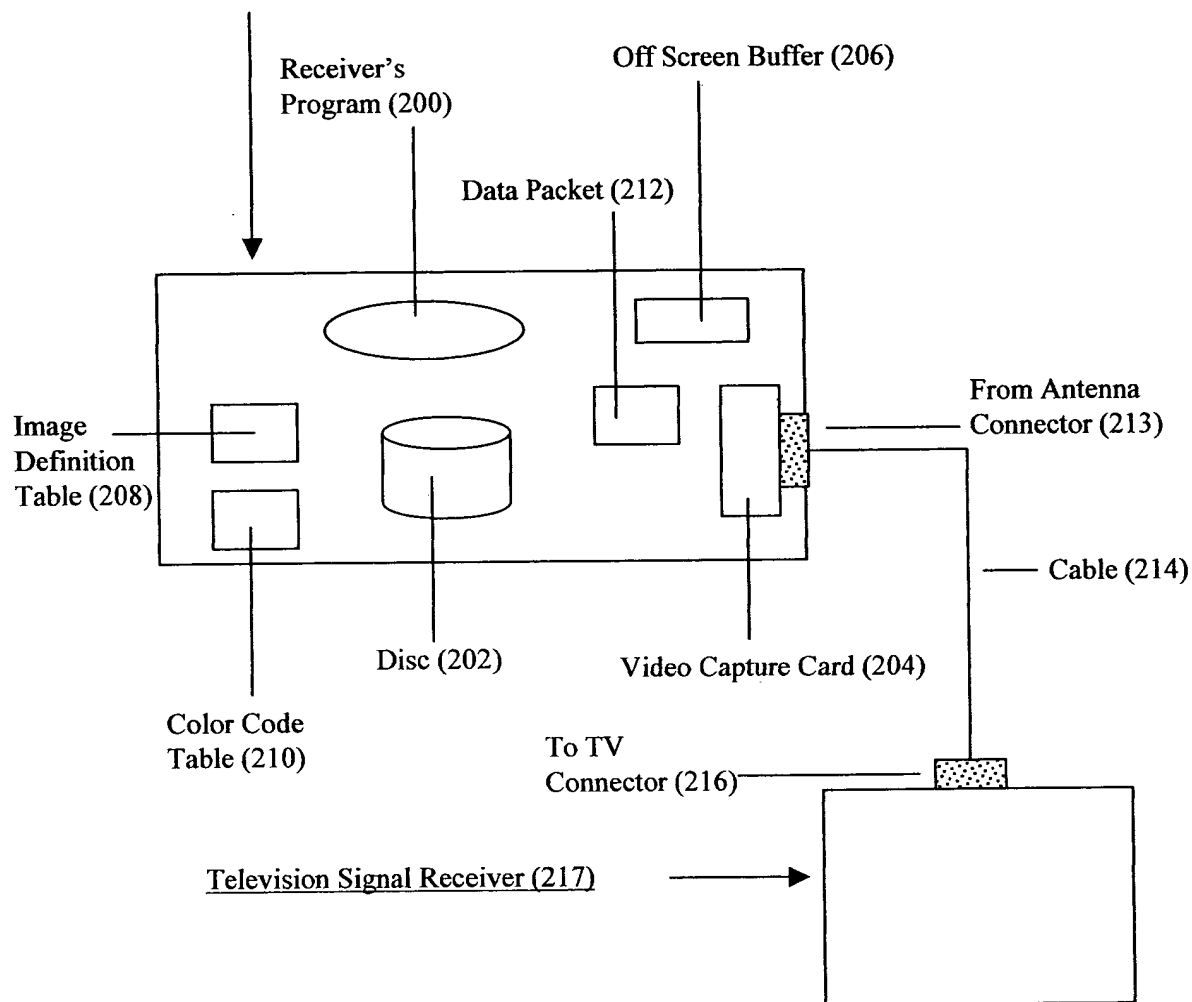


Fig. 9

10/16

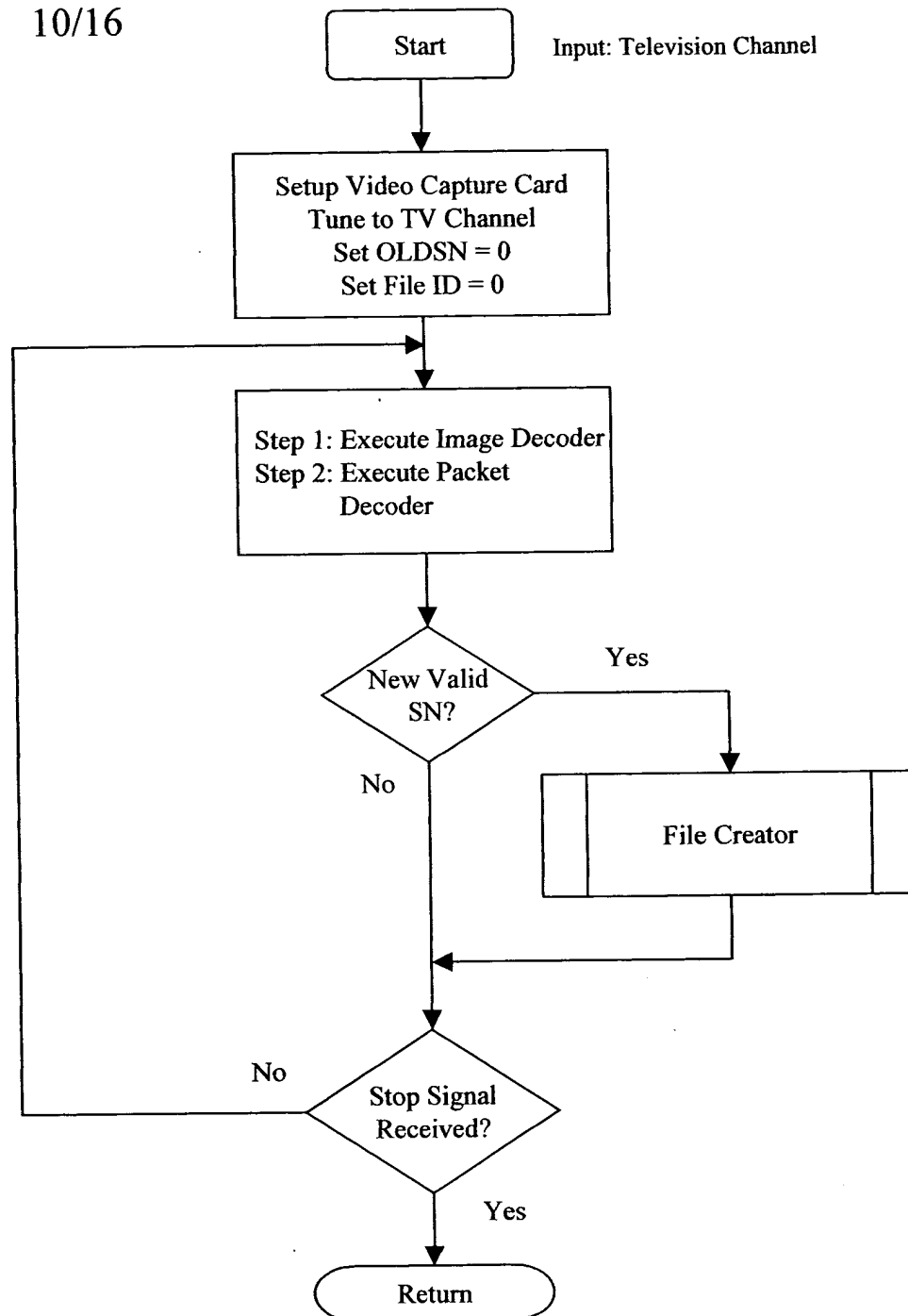


Fig. 10

11/16

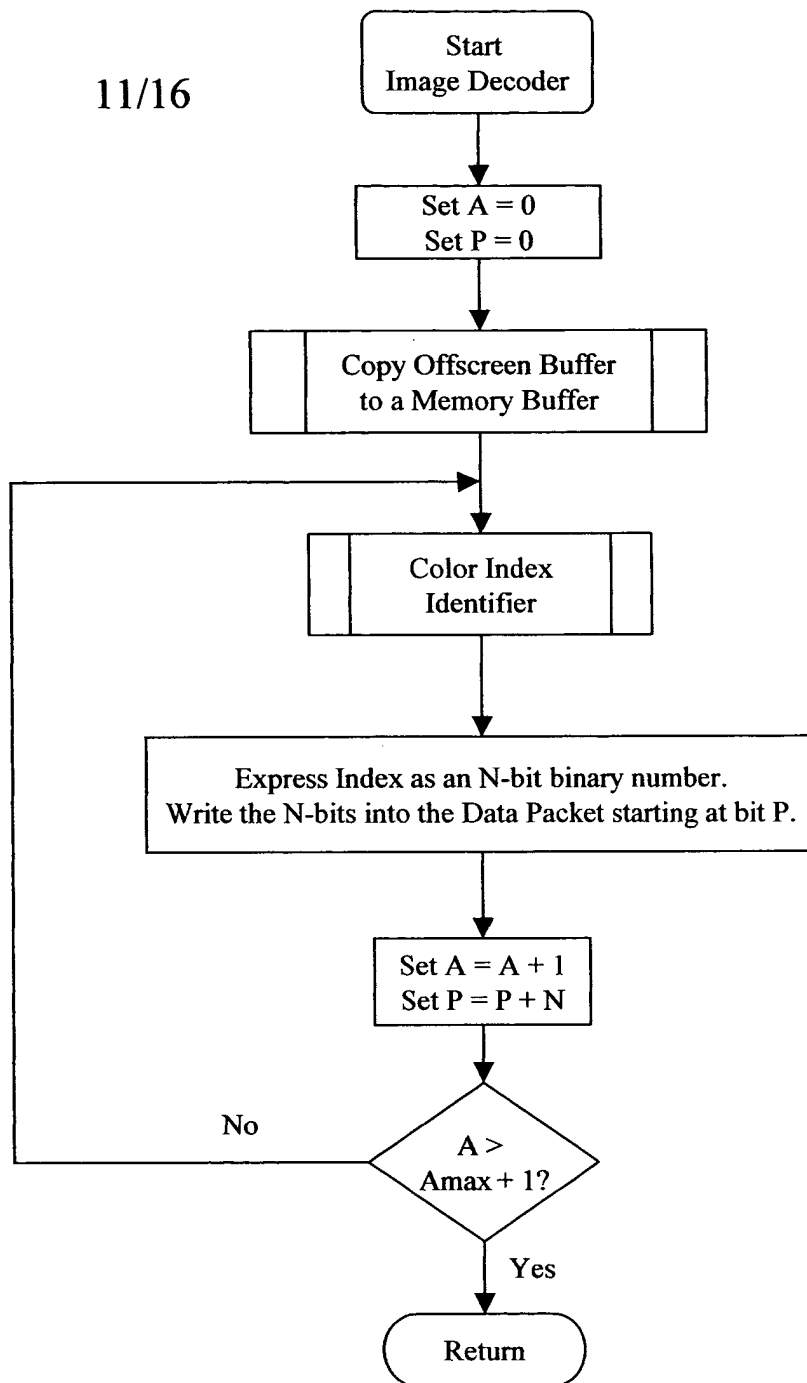


Fig. 11

12/16

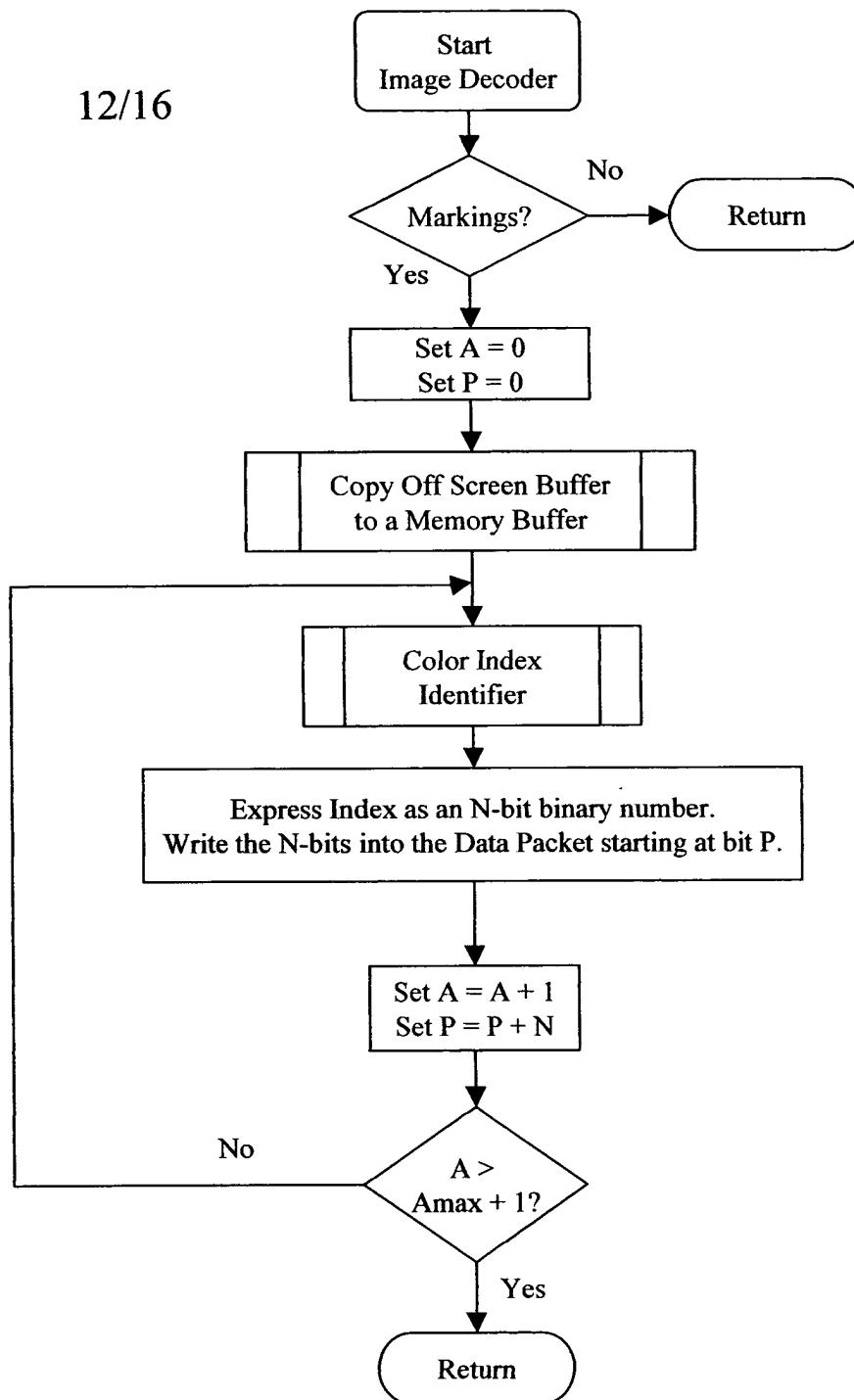


Fig. 11a

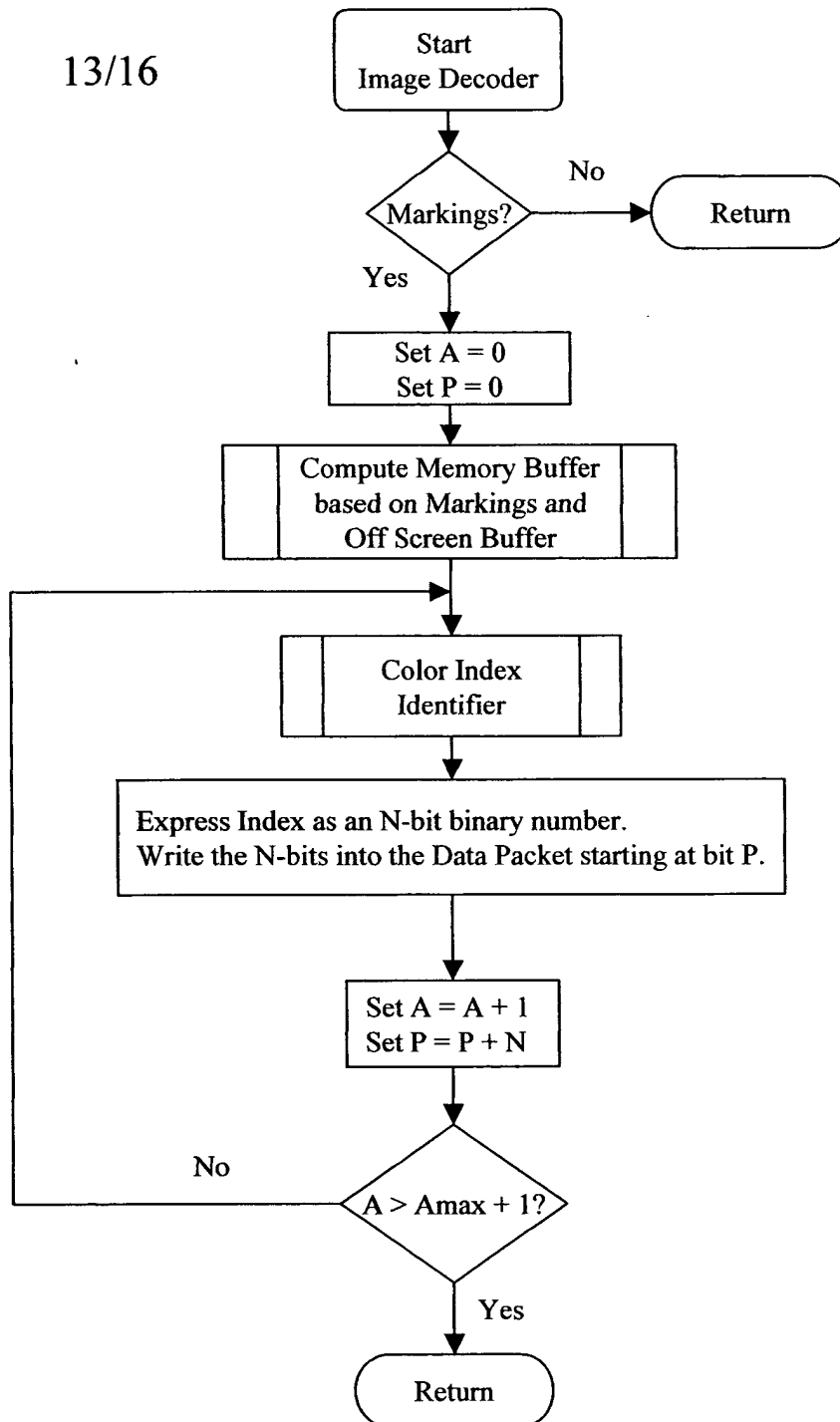


Fig. 11b

14/16

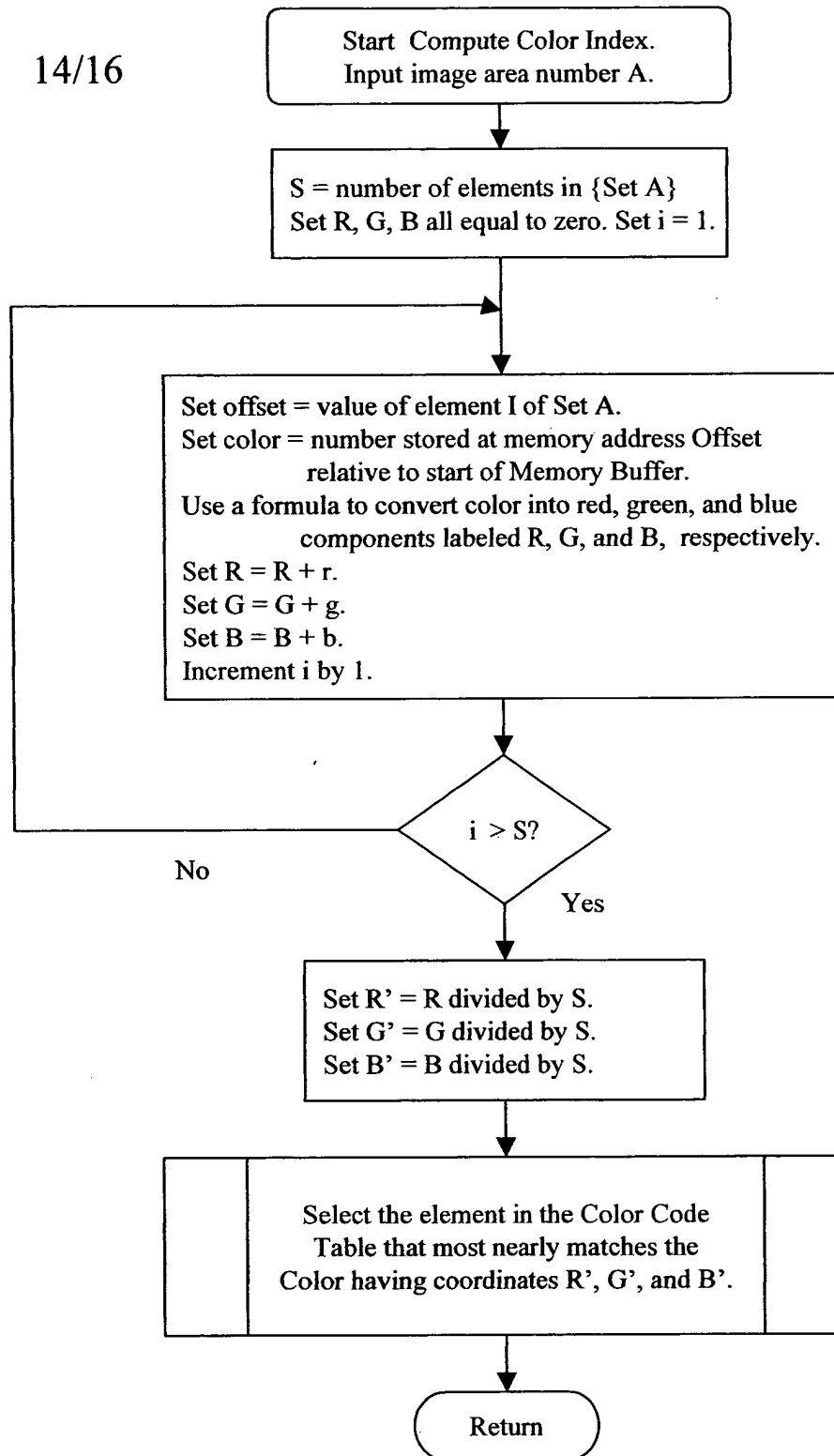


Fig. 12

15/16

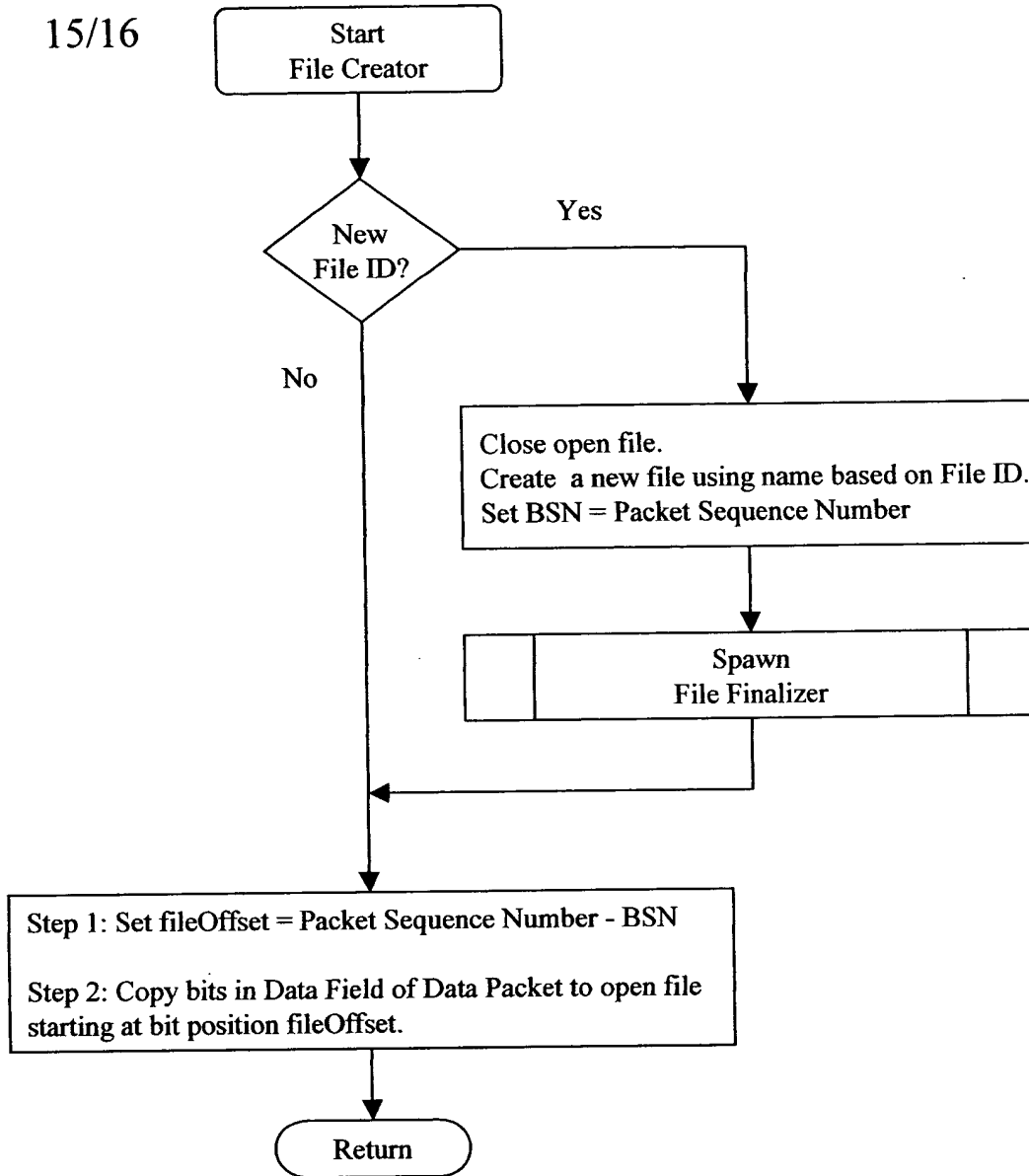


Fig. 13

16/16

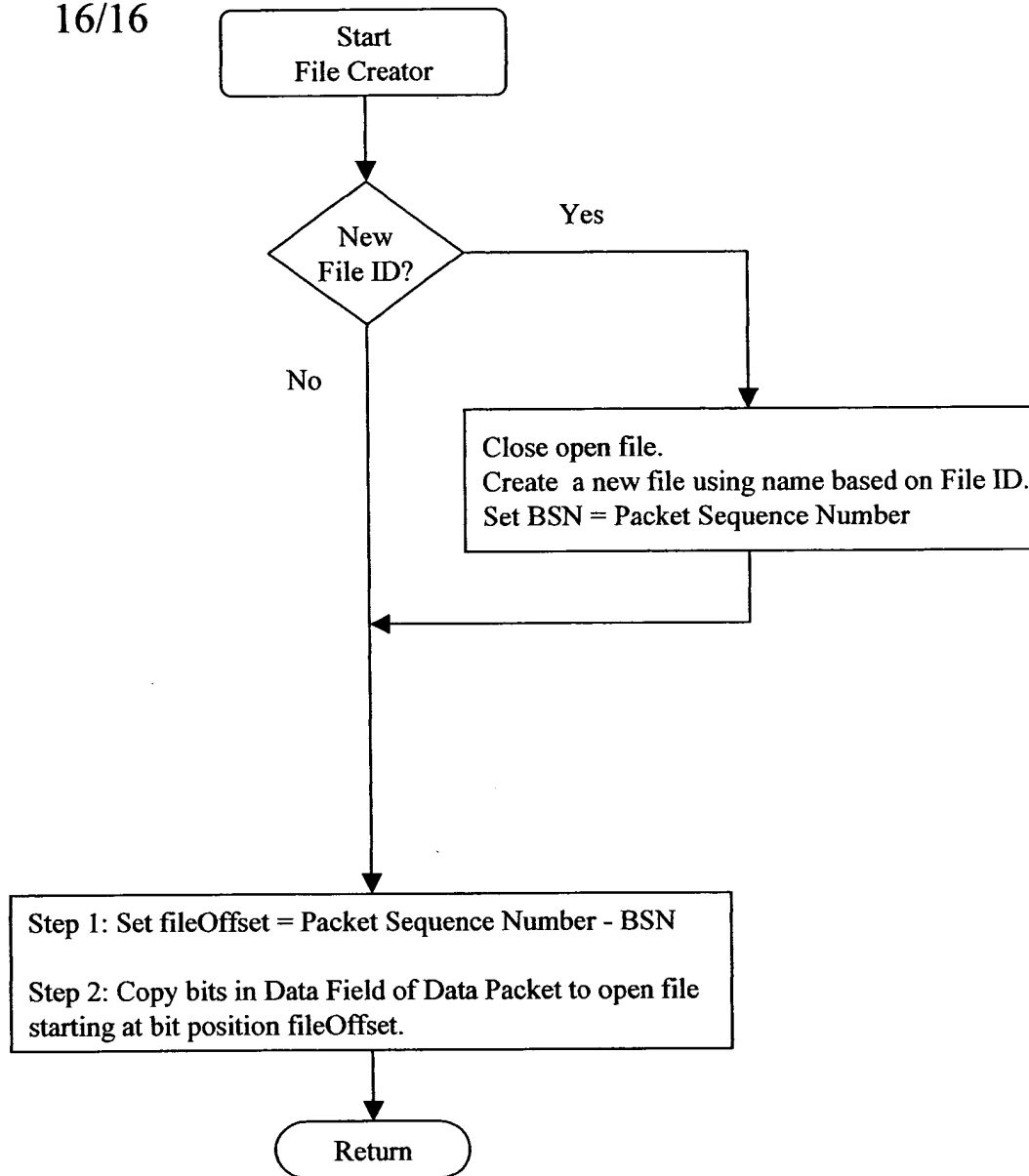


Fig. 13a